

Flash Memory Having a Flexible Bank Partition

ABSTRACT OF THE DISCLOSURE

A simultaneous operation flash memory chip architecture having a flexible
5 memory bank partition for forming first and second memory banks from a plurality of flash
memory arrays, said partition being defined by selecting one of a plurality of preformed
metal masks, which allows the formation and extension of pre-decoded address lines to inputs
of decoders associated with the first and second memory banks, respectively.

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